

**FIG. 1**

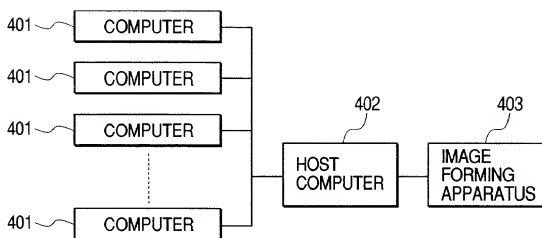


FIG. 2

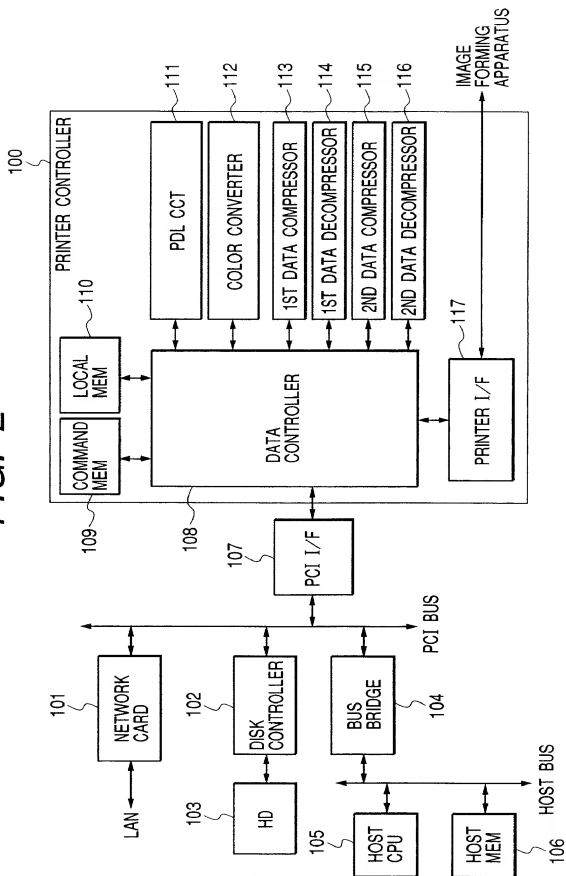


FIG. 3

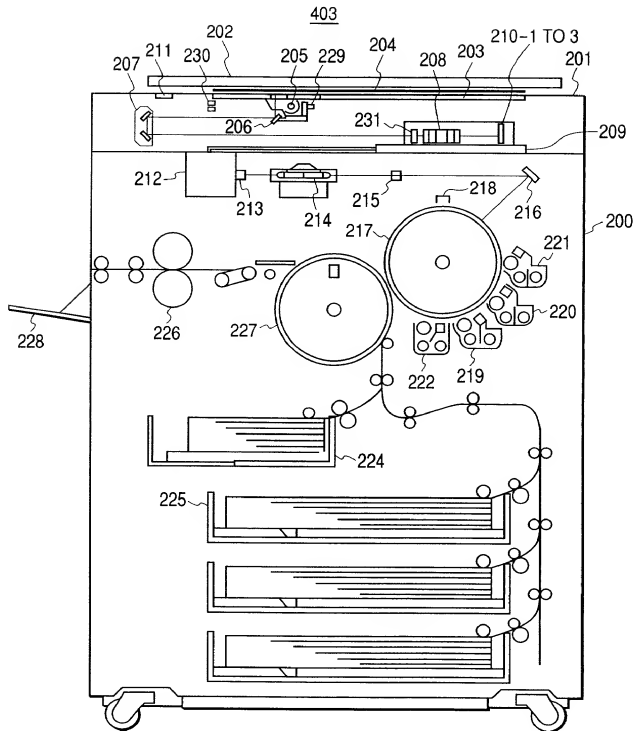
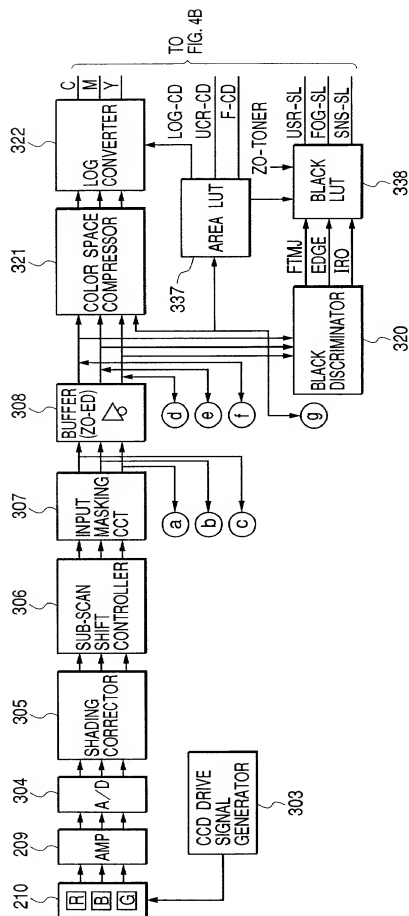


FIG. 4

FIG. 4A

FIG. 4A



[illegible]

The diagram illustrates a system architecture for image processing. At the top left, a logic block 301 contains a SUB-SCAN ADDRESS COUNTER and a MAIN-SCAN ADDRESS COUNTER. It receives inputs *l* and *m* via an AND gate, and input *n*. It outputs *LSYNC*, *VE*, and *PE* signals. A clock signal *VCLK* is provided to block 301 and a CPU 340. The CPU 340 is connected to RAM 342 and ROM 341. A control signal *302* is also connected to the CPU. On the left, a series of inputs *a* through *k* are fed into a FILTER 311. The output of the filter goes to a COLOR CONVERTER 312. Below the filter is a SHADE/OUTLINE GENERATOR 319, which receives input *319* and outputs *SC-BI* and *Z-BI* signals. An AREA GENERATOR 314 receives *SC-BI* and *Z-BI* signals and outputs an *AREA* signal. In the center, a SELECTOR (ZO-RGB) 318 receives inputs *e* through *h* and outputs to an INPUT MASKING CCT 315. Another SELECTOR (ZO-RGB) 316 receives inputs *i* and *h* and outputs to the same INPUT MASKING CCT 315. The INPUT MASKING CCT 315 outputs to an IMAGE SYNTHESIZER 317. The IMAGE SYNTHESIZER 317 receives inputs from the COLOR CONVERTER 312, the AREA GENERATOR 314, and the INPUT MASKING CCT 315. Its output goes to an I/F (Interface) block 313. The I/F block 313 also receives input *313* and outputs to the CPU 340.

FIG. 6

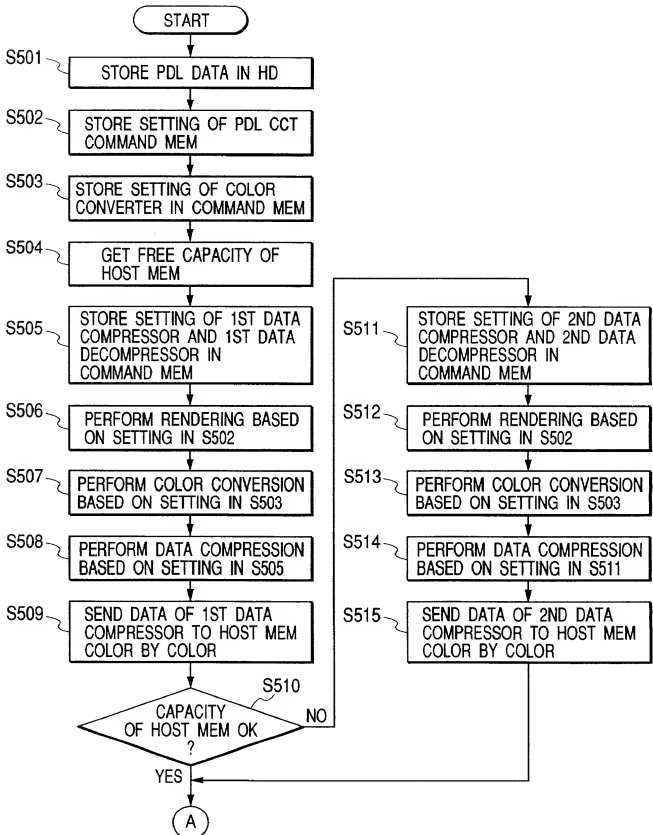


FIG. 7

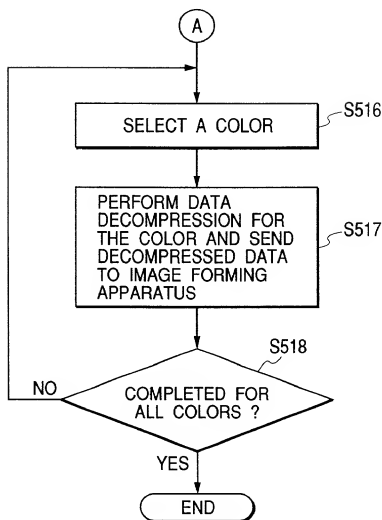


FIG. 8

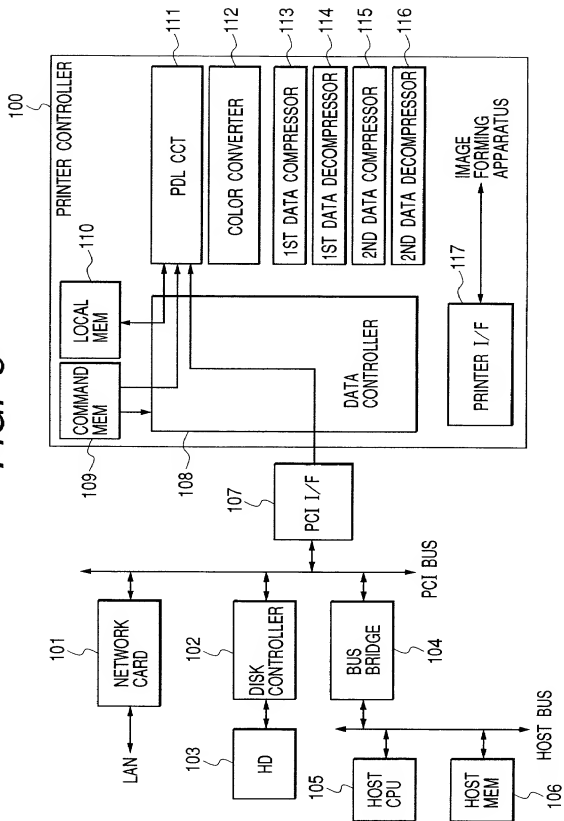


FIG. 9

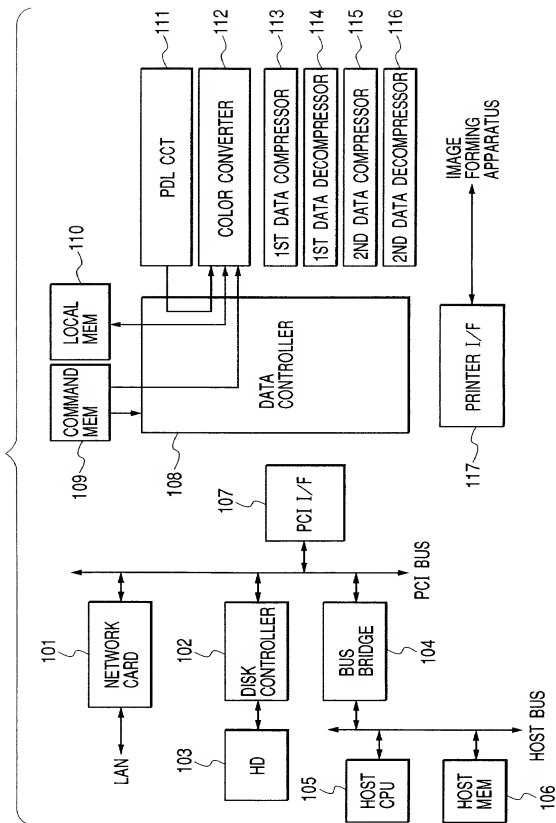


FIG. 10

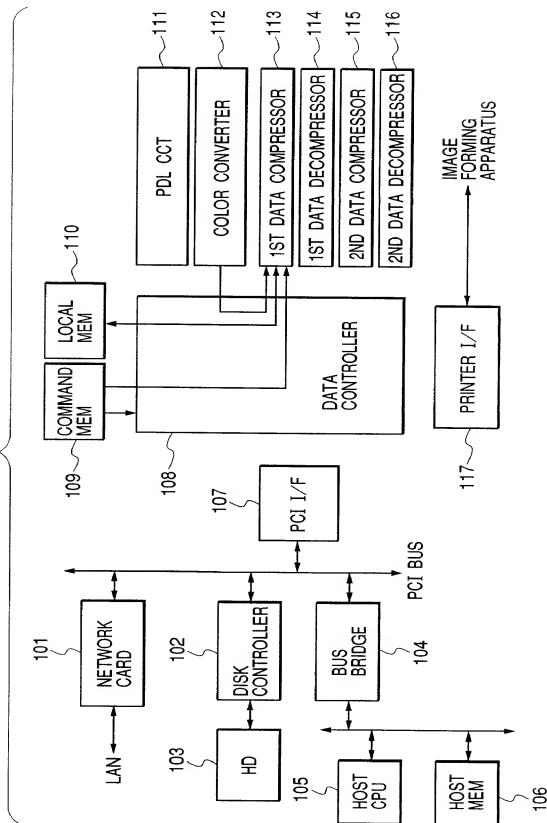


FIG. 11

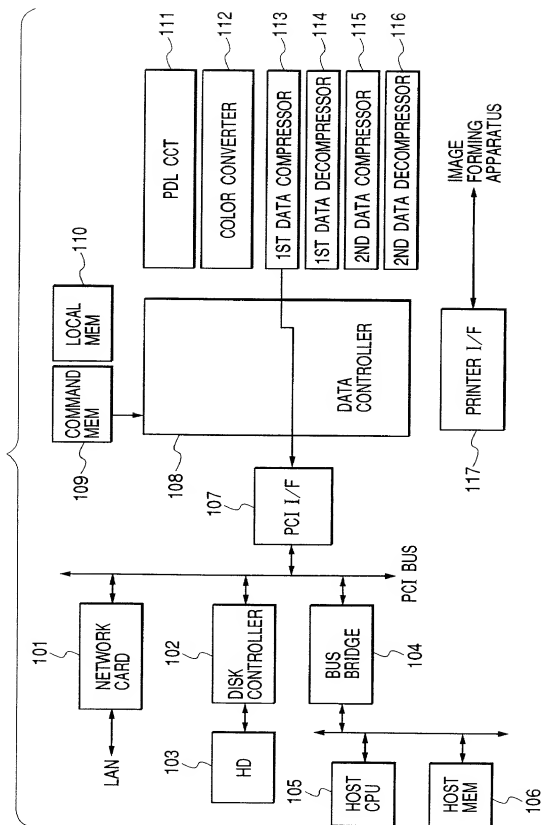


FIG. 12

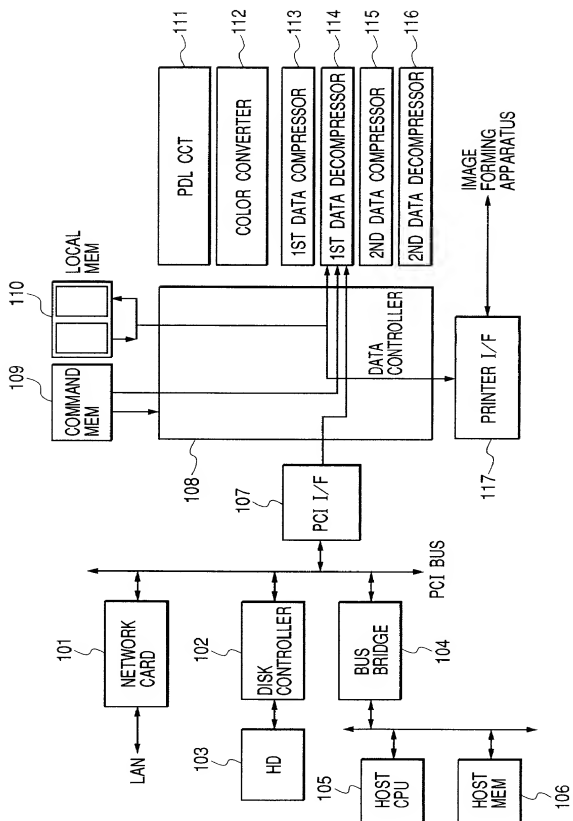
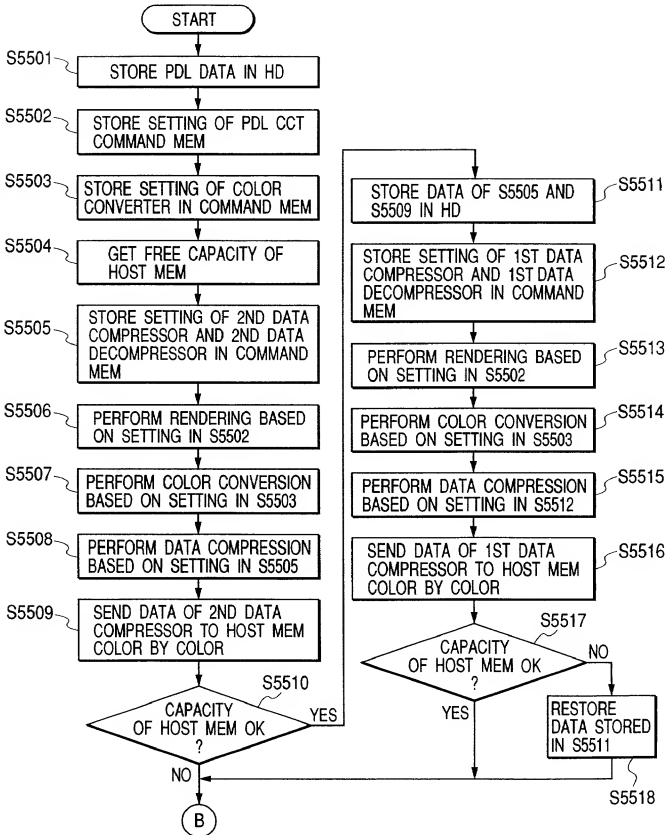
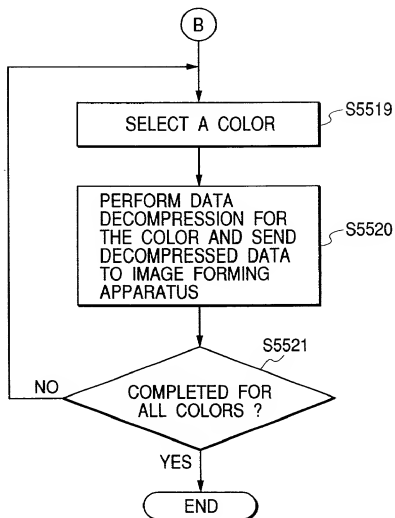


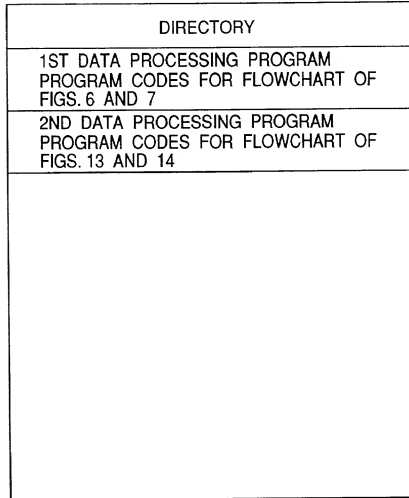
FIG. 13



**FIG. 14**

*FIG. 15*

MEMORY MAP OF MEM  
MEDIUM (FD/CD-ROM)

*FIG. 16*